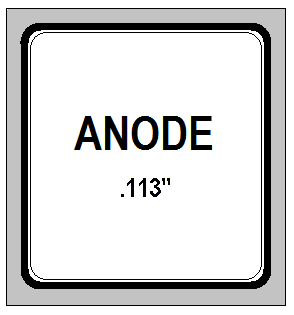
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**.135”**

**.135”**

**Top Material: Al**

**Backside Material: Ti/Ni/Ag**

**Bond Pad Size: .113” X .113”**

**Backside Potential: CATHODE**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .135” X .135” DATE: 9/21/21**

**MFG: ON SEMI THICKNESS .016” P/N: MURC1560**

**DG 10.1.2**

#### Rev B, 7/1